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STRAINED SEMICONDUCTOR BY FULL WAFER BONDING

REMARKS

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This responds to the Office Action dated on March 29, 2007.

Claims 1 and 16 are amended, no claims are canceled, and claims 66-69 are added; as a result, claims 1-53 and 66-69 are now pending in this application.

The present office action repeats the rejections found in the previous office action, adding a section entitled Response to Arguments. Applicant respectfully asserts that the previous arguments remain pertinent, and repeats those arguments below. Additionally, Applicant addresses, in the section directed to the §102 rejections, the Office's assertions regarding Clingman et al. and Belford found in the Response to Arguments.

§102 Rejection of the Claims

Claims 1-3, 6, 12, 16 and 18 were rejected under 35 U.S.C. § 102(e) as being anticipated by Clingman et al. (U.S. Patent No. 6,994,762). Applicant maintains its right to swear behind Clingman et al., but has chosen to distinguish the claim over the reference. Statements distinguishing the claimed subject matter over Clingman et al. are not to be interpreted as admission that the Clingman et al. is prior art. Applicant respectfully traverses for at least the following reasons.

The rejection refers to element 14 in Clingman as a substrate wafer. Applicant disagrees. Clingman refers to element 14 as a steel layer, which Applicant submits is not a substrate wafer. The terms substrate and wafer refer generally to any structure on which integrated circuits are formed, and also to such structures during various stages of integrated circuit fabrication (Applicant's Specification at page 6 line 23 ff.). Steel is not a material on which integrated circuits are formed. The piezo material is adhered to the steel layer 14 using adhesive 16 when the steel layer is flexed, which Clingman indicates allows the piezo material to not fracture when the structure (including the steel layer 14) is placed in tension during aerodynamic flow control and structural energy harvesting applications (col. 1 lines 51-60).

Regarding the Office's Response to Applicant's previous arguments concerning Clingman et al., the Office states: However, in column 2 at line 65, Clingman et al. teach the steel layer (14) may be a substrate. Applicant respectfully submits that this section of Clingman Serial Number: 10/623,788 Filing Date: July 21, 2003

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et al. indicates that a layer of SCP material is bonded to a steel layer or substrate 14. Applicant respectfully submits that one of ordinary skill would interpret the term "substrate" in this sentence to be an alternative term for steel layer --- not a separate structure. In support of Applicant's position, Applicant notes that "14" is used in Clingman et al. to identify substrate at column 2 lines 65, and that "14" is used to identify steel structure elsewhere (e.g. col. 2 line 66). Further, Applicant asserts that the claims refer to "substrate wafer". Applicant cannot find a showing or suggestion that the steel layer 14 in Clingman et al. is a wafer.

Applicant acknowledges that, during patent examination, the claims are given the broadest reasonable interpretation consistent with the specification. However, Applicant respectfully submits that interpreting a substrate wafer to be a steel layer is not consistent with the specification, and thus is not a reasonable interpretation.

However, in an effort to advance prosecution beyond this issue, Applicant has chosen to amend independent claims 1 and 16 to clarify that the substrate wafer is a structure used in integrated circuit fabrication on which integrated circuits are formed. No new matter is added. Applicant submits the amendment is supported at least at page 6 lines 23 ff. Steel is a conductor which is not used as a substrate in integrated circuit fabrication -- integrated circuits are not formed on steel substrates.

Regarding independent claim 1, Applicant respectfully asserts that Clingman et al. does not show a method for forming a wafer as recited in the claim. Applicant is unable to find a semiconductor membrane bonded to a substrate wafer, as recited in the claim, where the substrate wafer is a structure used in integrated circuit fabrication on which integrated circuits are formed. Applicant submits the steel layer 14 of Clingman et al. is not a substrate wafer. Applicant asserts claim 1 is in condition for allowance. Claims 2-3, 6 and 12 depend on claim 1, and are asserted to be in condition for allowance at least for the reasons provided with respect to claim 1.

Regarding independent claim 16, Applicant respectfully asserts that Clingman et al. does not show a method for forming a wafer, as recited in the claim, where the substrate wafer is a structure used in integrated circuit fabrication on which integrated circuits are formed. Applicant is unable to find a portion of the substrate wafer bonded to a semiconductor layer when the substrate wafer is in the flexed position. Applicant submits the steel layer 14 of Clingman et al.

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is not a substrate wafer. Applicant asserts claim 16 is in condition for allowance. Claim 18 depends on claim 16, and is asserted to be in condition for allowance at least for the reasons provided with respect to claim 16.

Claims 28 and 29 were rejected under 35 U.S.C. § 102(e) as being anticipated by Belford (U.S. Patent No. 6,514,836). Applicant maintains its right to swear behind Belford, but has chosen to distinguish the claim over the reference. Statements distinguishing the claimed subject matter over Clingman et al. are not to be interpreted as admission that the Clingman et al. is prior art. Applicant respectfully traverses for at least the following reasons.

Regarding the Office's Response to Applicant's previous arguments concerning Belford, the Office states: Applicant argues Belford does not teach performing a bond cut to a flexed region of a substrate. However, Belford discloses a strained region, in its broadest interpretation, flexing a region creates a strain. Belford discloses using the bond cut (smart cut) to a strained silicon on insulator, applicant claims a method for forming a wafer, this may includes a silicon-on-insulator wafer. Applicant respectfully traverses, respectfully submitting that the office's response mischaracterizes Applicant's arguments, and is unclear.

The rejection relies on two distinct embodiments in Belford, and Belford neither shows nor suggests that these embodiments can be used together. Further, as is discussed below, Applicant respectfully asserts that the two distinct embodiments cannot be used together. As such, Belford does not anticipate the claim, because Belford does not show the elements of the claim arranged as required by the claim.¹

One distinct embodiment is illustrated in FIG. 2 where a sheet is bonded to a membrane to induce uniaxial strain when the membrane 202 and thicker sheet 206 are released from the curve support (Col. 3 lines 16-32). Another distinct embodiment refers to biaxial strains using differential thermal bonding (FIGS. 3-5; Col. 3 line 36 ff.). FIGS. 6-8 are referenced when

¹ "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson* v. *Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). MPEP 2131.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.116 – EXPEDITED PROCEDURE

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stating that standard SOI techniques can be used along with Differential Thermal Bonding Techniques to induce biaxial strain (Col. 3 lines 52-54). The SMART CUT process is identified with respect to the thermal bonding process (Col. 3 lines 63-67; THE SOI method employed is called "SMART CUT" combining this method with differential thermal bonding is a effective way of creating strained Si on insulator (SSOI)). The thermal bonding process does not involve flexing the substrate. Further, the SMART CUT technique is not disclosed with a techniques that flexes the substrate. Thus, Belford does not show the claimed subject matter in as complete detail as contained in the claim because the rejection relies on two distinct embodiments and Belford neither shows nor suggests these distinct embodiments as being used together. Applicant further asserts, for reasons provided below, that these distinct embodiments cannot be used together. Therefore, Belford does not anticipate the claim.

It appears that the Office's response may be attempting to assert that the thermal bonding "flexes" the central region of a substrate wafer into a flexed position. However, assuming for the sake of argument that the central region is flexed into a flexed position during thermal bonding, it is unclear what portion of Belford is being relied upon to show that, after the bond cut process, the substrate wafer is relaxed to induce a predetermined strain in the silicon membrane. Again, Applicant asserts that the bond cut process is only discussed with respect to the second embodiment (thermal bonding), and is not discussed with respect to the first embodiment. In the first embodiment, the thickness of the Si layer 104 is thinned by CMP, grinding, lapping, polishing, and/or etching (col. 3 lines 13-15) before the thinned Si layer is placed face down over the curvature of support structure 204 (col. 3 lines 19-25), then bonded to a thicker sheet 206(col. 3 lines 23-27, and then released from the curved support (col. 3 lines 28-30). In the bond cut process, the bond is created before the bulk of the substrate is cracked off (col. 3 lines 55-65). Applicant submits that the bulk substrate is not thin enough to be curved or flexed over the curvature of the support structure. Also, the membrane is not bonded to the curved support structure, so it is unclear how the bulk of substrate would crack off during the bond cut process.

With respect to independent claim 28, Applicant is unable to find in Belford a method for forming a wafer, comprising, among other things, performing a bond cut process to form a silicon membrane from a crystalline sacrificial wafer and bond a peripheral region of the substrate wafer to a peripheral region of a silicon membrane when the substrate wafer is in the

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flexed position, as recited in the claim. Further, Applicant is unable to find where the substrate wafer is relaxed to induce a predetermined strain in the silicon membrane after the bond cut process is performed. Applicant respectfully requests withdrawal of the rejection, and reconsideration and allowance of independent claim 28. Claim 29 depends on claim 28 and is asserted to be in condition for allowance for at least the reasons provided with respect to claim 28.

§103 Rejection of the Claims

Claims 4, 9-11, 17, 19 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Clingman et al. (U.S. Patent No. 6,994,762) in view of Belford (U.S. Patent No. 6,514,836). Applicant respectfully traverses. The proposed addition of Belford to Clingman does not remedy the deficiencies of the rejection made with respect to Clingman, as identified above. Claims 4, and 9-11 depend on claim 1, and are asserted to be in condition for allowance at least for the reasons provided with respect to claim 1. Claims 17 and 19-20 depend on claim 16, and are asserted to be in condition for allowance at least for the reasons provided with respect to claim 16.

Claims 5, 21, 39-41, 44-46 and 53 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Clingman et al. (U.S. Patent No. 6,994,762) in view of Belford (U.S. Patent No. 6,514,836) and Yamazaki et al. (U.S. Patent No. 6,902,616). Applicant respectfully traverses. The proposed addition of Belford and Yamazaki to Clingman does not remedy the deficiencies of the rejection made with respect to Clingman, as identified above. Claim 5 depends on claim 1, and is asserted to be in condition for allowance at least for the reasons provided with respect to claim 1. Claim 21 depends on claim 16, and is asserted to be in condition for allowance at least for the reasons

With respect to independent claim 39, Applicant is unable to find, among other things, in the suggested combination of Clingman, Belford and Yamazaki a showing or suggestion of a method for forming a wafer where a convex contour is formed in a surface of a sacrificial crystalline wafer, and a bond cut process is performed to form an ultra-thin semiconductor membrane and bond the ultra-thin semiconductor membrane to a substrate wafer, where the

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ultra-thin semiconductor membrane is flattened and strained when bonded to the substrate wafer, as recited in the claim. Applicant submits there is no suggestion to use a bond cut process with a contoured surface, and further submits that Yamazaki does not show a sacrificial crystalline wafer, as recited in the claim. Claims 40-41 depend on claim 39 and are asserted to be in condition for allowance at least for the reasons provided with respect to claim 39.

With respect to independent claim 44, Applicant is unable to find, among other things, in the suggested combination of Clingman, Belford and Yamazaki a showing or suggestion of a method for forming a transistor comprising, among other things, forming a predetermined contour in one of a semiconductor layer and a substrate wafer, and bonding the semiconductor layer to the substrate wafer and straightening the predetermined contour to induce a predetermined strain in the semiconductor layer, as recited in the claim. The proposed combination of Belford and Yamazaki do not remedy the deficiencies of the rejections in view of Clingman as identified above. Claims 45-46 depend on claim 44 and are asserted to be in condition for allowance at least for the reasons provided with respect to claim 44.

With respect to independent claim 53, Applicant is unable to find, among other things, in the suggested combination of Clingman, Belford and Yamazaki a showing or suggestion of a method for forming an electronic system comprising, among other things, forming a predetermined contour in one of a semiconductor layer and a substrate wafer, and bonding the semiconductor layer to the substrate wafer and straightening the predetermined contour to induce a predetermined strain in the semiconductor layer, as recited in the claim. The proposed combination of Belford and Yamazaki do not remedy the deficiencies of the rejections in view of Clingman as identified above.

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Allowable Subject Matter

Applicant thanks the examiner for the finding of allowable subject matter.

Claims 22-27, 31-38 and 47-52 were allowed.

Claims 8, 15, 30 and 42 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. New claim 66 includes language recited in original claims 1, 6 and 8. New claim 67 includes language recited in original claims 1 and 15. New claim 68 includes language recited in original claims 28 and 29, and previously-presented claim 30. New claim 69 includes language recited in original claims 39 and 42. Applicant respectfully requests allowance of new claims 66-69.

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CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6960 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 2007.

Name

Signature